ECP103

1 Watt, High Linearity InGaP HBT Amplifier

The Communications Edge ™

Product Information

Product Features

- 2300 - 2700 MHz
- +31 dBm P1dB
- +47 dBm Output IP3
- 11.5 dB Gain @ 2450 MHz
- 10 dB Gain @ 2650 MHz
- Single Positive Supply (+5V)
- Available in 16pin 4mm QFN and Lead-free/green/RoHS-compliant SOIC-8 packages

Applications

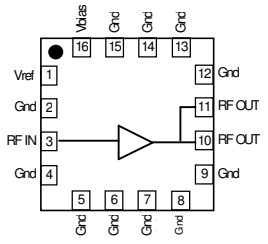
- W-LAN / Wi-Bro
- RFID
- DMB
- Fixed Wireless

Product Description

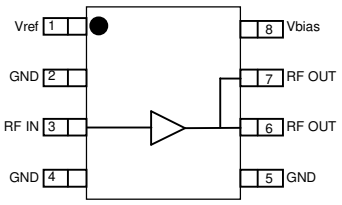
The ECP103 is a high dynamic range driver amplifier in a low-cost surface mount package. The InGaP/GaAs HBT is able to achieve superior performance for various narrowband-tuned application circuits with up to +47 dBm OIP3 and +31 dBm of compressed 1-dB power. It is housed in a 16-pin 4x4mm QFN and Lead-free/ green/RoHS-compliant SOIC-8 SMT packages. All devices are 100% RF and DC tested.

The ECP103 is targeted for use as a driver amplifier in wireless infrastructure where high linearity and medium power is required. An internal active bias allows the ECP103 to maintain high linearity over temperature and operate directly off a single +5V supply. This combination makes the device an excellent candidate for driver amplifier stages in wireless-LAN, digital multimedia broadcast, or fixed wireless applications. The device can also be used in next generation RFID readers.

Functional Diagram



ECP103D



ECP103G / ECP103G-G

Specifications (1)

Parameter	Units	Min	Typ	Max
Operational Bandwidth	MHz	2300		2700
Test Frequency	MHz		2450	
Gain	dB	9	11.5	
Input Return Loss	dB		12	
Output Return Loss	dB		22	
Output P1dB	dBm	29.5	+31	
Output IP3 (2)	dBm	44.5	+47	
Noise Figure	dB		6.3	
Test Frequency	MHz		2650	
Gain	dB		10	
Output P1dB	dBm		+30.5	
Output IP3 (2)	dBm		+48	
Operating Current Range , Icc (3)	mA	400	450	500
Device Voltage, Vcc	V		5	

1. Test conditions unless otherwise noted: T = 25ºC, Vsupply = +5 V in a tuned application circuit.
2. 3OIP measured with two tones at an output power of +15 dBm/tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the 3OIP using a 2:1 rule.
3. This corresponds to the quiescent current or operating current under small-signal conditions into the Vbias and RF out pins. It is expected that the current can increase by an additional 90 mA at P1dB. Pin 1 is used as a reference voltage for the internal biasing circuitry. It is expected that Pin 1 will pull 10.8 mA of current when used with a series bias resistor of R1=51 Ω. (ie. total device current typically will be 461 mA.)

Typical Performance (4)

Parameter	Units	Typical		
Frequency	MHz	2350	2450	2650
S21 – Gain	dB	12	11.5	10
S11	dB	-11.5	-12	-25
S22	dB	-16.5	-22	-8.5
Output P1dB	dBm	31	31	30.5
Output IP3	dBm	45	47	48
Noise Figure	dB	6.3	6.3	6.3
Supply Bias (3)		+5 V @ 450 mA		

4. Typical parameters reflect performance in a tuned application circuit at +25° C.

Absolute Maximum Rating

Parameter	Rating
Operating Case Temperature	-40 to +85 °C
Storage Temperature	-65 to +125 °C
RF Input Power (continuous)	+26 dBm
Device Voltage	+8 V
Device Current	900 mA
Device Power	5 W
Junction Temperature	+250 °C

Operation of this device above any of these parameters may cause permanent damage.

Ordering Information

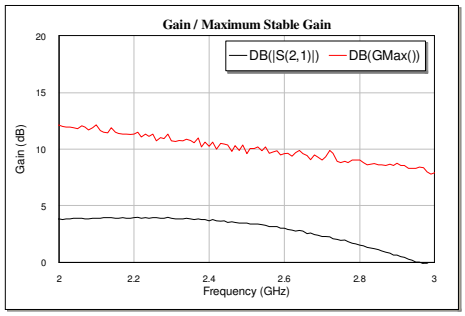
Part No.	Description
ECP103D	1 Watt InGaP HBT Amplifier (lead-tin 16p 4x4mm Pkg)
ECP103G*	1 Watt InGaP HBT Amplifier (lead-tin SOIC-8 Pkg)
ECP103G-G	1 Watt InGaP HBT Amplifier (lead-free/green/RoHS-compliant SOIC-8 Pkg)
ECP103D-PCB2450	2450 MHz Evaluation Board
ECP103D-PCB2650	2650 MHz Evaluation Board
ECP103G-PCB2450	2450 MHz Evaluation Board
ECP103G-PCB2650	2650 MHz Evaluation Board

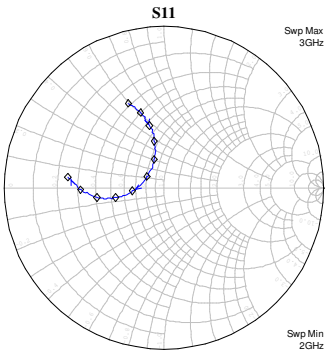
* This package is being phased out in favor of the green package type which is backwards compatible for existing designs. Refer to Product Change Notification WJPCN06MAY05TC1 on the WJ website.

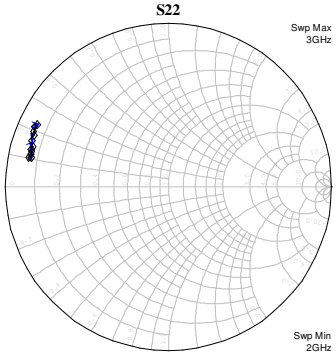
Specifications and information are subject to change without notice

Typical Device Data (QFN 4 X 4)

S-Parameters (V_{CC} = +5 V, I_{CC} = 450 mA, T = 25°C, unmatched 50 ohm system)





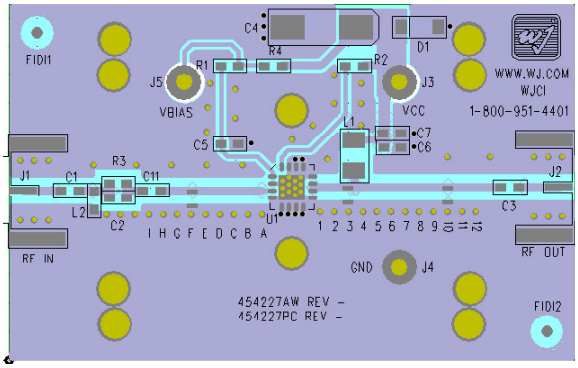


Notes:
The gain for the unmatched device in 50 ohm system is shown as the trace in black color. For a tuned circuit for a particular frequency, it is expected that actual gain will be higher, up to the maximum stable gain. The maximum stable gain is shown in the dashed red line. The impedance plots are shown from 2 – 3 GHz, with markers placed at 2.0 – 3.0 GHz in 0.1 GHz increments.

S-Parameters (V_{CC} = +5 V, I_{CC} = 450 mA, T = 25°C, unmatched 50 ohm system, calibrated to device leads)

Freq (GHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
2	-4.91	113.13	3.83	18.85	-32.93	-51.51	-1.33	168.01
2.1	-6.24	107.44	3.91	10.89	-33.48	-65.58	-1.17	168.11
2.2	-8.08	103.30	3.95	1.80	-33.11	-69.18	-1.25	166.73
2.3	-10.62	101.88	3.87	-8.34	-32.53	-79.53	-1.26	165.64
2.4	-14.63	108.84	3.69	-18.36	-33.55	-93.98	-1.20	164.67
2.5	-17.90	146.99	3.45	-29.22	-32.21	-97.59	-1.27	163.61
2.6	-14.09	-174.72	3.00	-40.69	-33.90	-111.38	-1.10	161.41
2.7	-10.21	-168.94	2.29	-52.48	-35.64	-110.30	-1.11	159.01
2.8	-7.47	-171.72	1.51	-63.22	-36.47	-135.22	-0.98	157.77
2.9	-5.66	-178.73	0.63	-74.29	-36.22	-145.07	-0.93	155.95
3	-4.36	173.71	-0.41	-83.23	-37.26	-153.27	-1.05	154.63

Application Circuit PC Board Layout



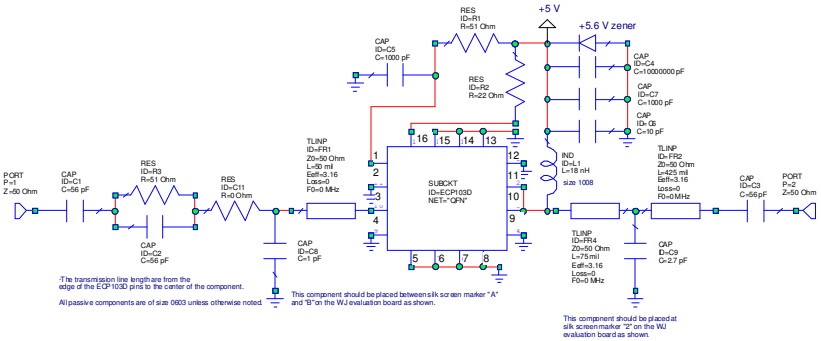
Circuit Board Material: .014" Getek, single layer, 1 oz copper, Microstrip line details: width = .026", spacing = .026"
The silk screen markers 'A', 'B', 'C', etc. and '1', '2', '3', etc. are used as placemarkers for the input and output tuning shunt capacitors – C8 and C9. The markers and vias are spaced in .050" increments.

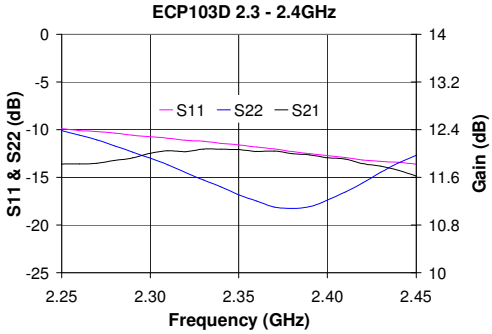
2350 MHz Reference Design

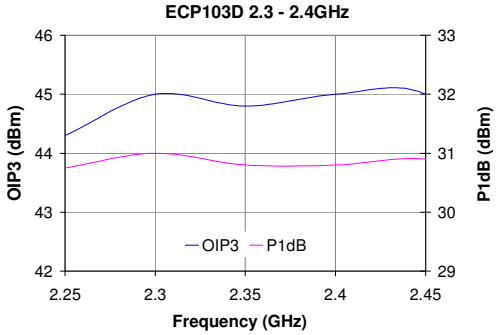
Typical RF Performance at 25°C

Frequency	2350 MHz
S21 – Gain	12 dB
S11 – Input Return Loss	-11.5 dB
S22 – Output Return Loss	-16 dB
Output P1dB	+31 dBm
Output IP3 (+15 dBm / tone, 1 MHz spacing)	+45 dBm
Noise Figure	6.3 dB
Device / Supply Voltage	+5 V
Quiescent Current (1)	450 mA

1. This corresponds to the quiescent current or operating current under small-signal conditions into pins 10, 11, and 16.





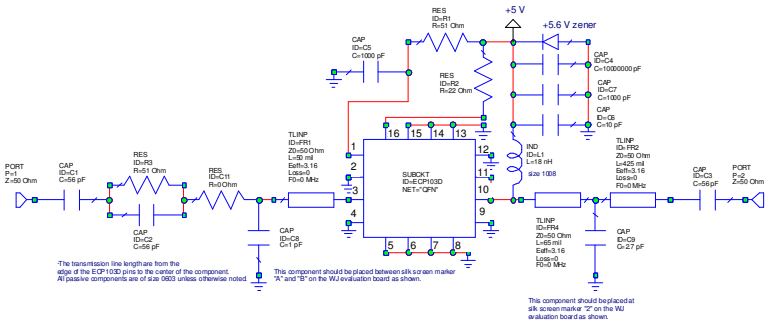


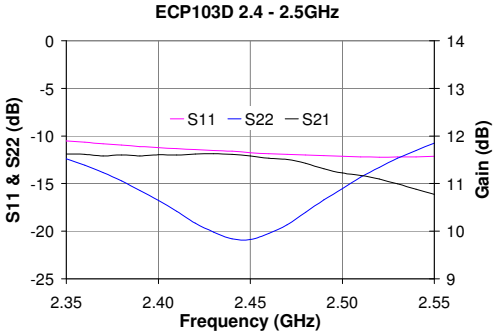
2450 MHz Application Circuit (ECP103D-PCB2450)

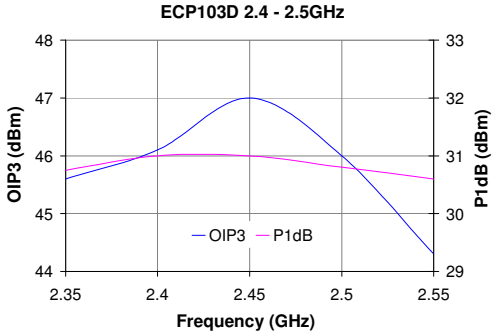
Typical RF Performance at 25°C

Frequency	2450 MHz
S21 – Gain	11.5 dB
S11 – Input Return Loss	-12 dB
S22 – Output Return Loss	-22 dB
Output P1dB	+31 dBm
Output IP3 (+15 dBm / tone, 1 MHz spacing)	+47 dBm
Noise Figure	6.3 dB
Device / Supply Voltage	+5 V
Quiescent Current (1)	450 mA

1. This corresponds to the quiescent current or operating current under small-signal conditions into pins 10, 11, and 16.





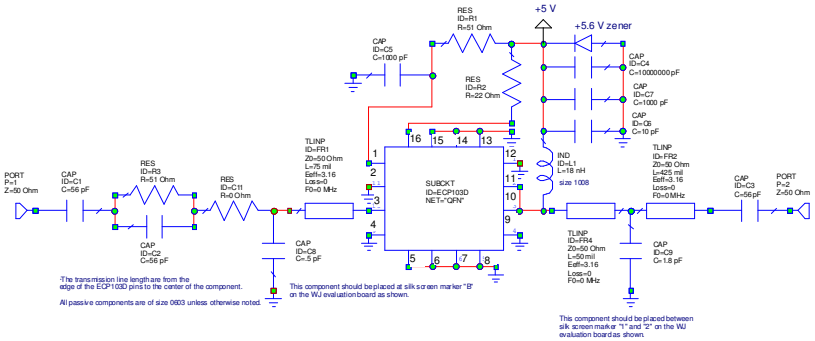


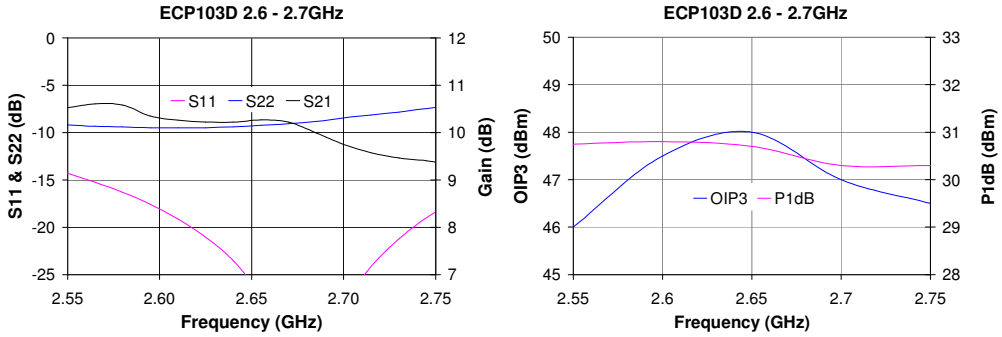
2650 MHz Application Circuit (ECP103D-PCB2650)

Typical RF Performance at 25°C

Frequency	2650 MHz
S21 – Gain	10 dB
S11 – Input Return Loss	-25 dB
S22 – Output Return Loss	-8.5 dB
Output P1dB	+30.5 dBm
Output IP3 (+15 dBm / tone, 1 MHz spacing)	+48 dBm
Noise Figure	6.3 dB
Device / Supply Voltage	+5 V
Quiescent Current (1)	450 mA

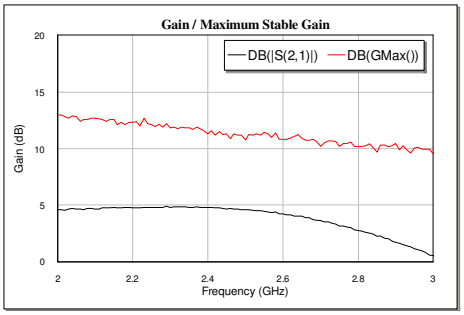
1. This corresponds to the quiescent current or operating current under small-signal conditions into pins 10, 11, and 16.

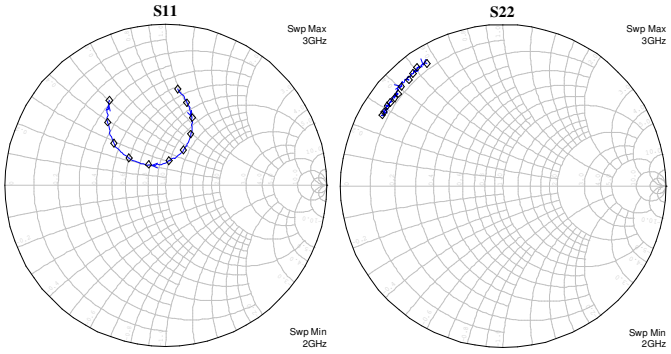




Typical Device Data (SOIC-8)

S-Parameters (V_{CC} = +5 V, I_{CC} = 450 mA, T = 25°C, unmatched 50 ohm system)



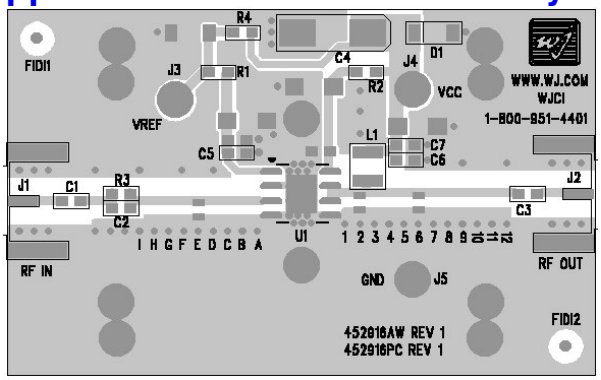


Notes:
The gain for the unmatched device in 50 ohm system is shown as the trace in black color. For a tuned circuit for a particular frequency, it is expected that actual gain will be higher, up to the maximum stable gain. The maximum stable gain is shown in the dashed red line. The impedance plots are shown from 2 – 3 GHz, with markers placed at 2.0 – 3.0 GHz in 0.1 GHz increments.

S-Parameters (V_{CC} = +5 V, I_{CC} = 450 mA, T = 25°C, unmatched 50 ohm system, calibrated to device leads)

Freq (GHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
2	-4.42	82.96	4.60	-0.51	-34.32	-55.22	-1.27	149.42
2.1	-5.52	75.86	4.66	-9.34	-33.36	-64.33	-1.26	147.91
2.2	-6.91	68.62	4.76	-19.13	-34.27	-69.46	-1.22	145.11
2.3	-9.01	64.17	4.83	-30.17	-34.14	-88.95	-1.26	143.35
2.4	-12.19	63.53	4.80	-41.46	-34.25	-111.58	-1.29	140.76
2.5	-16.19	82.79	4.61	-54.22	-35.82	-117.53	-1.28	138.47
2.6	-15.51	129.26	4.24	-68.07	-34.41	-143.18	-1.12	135.41
2.7	-10.94	143.17	3.65	-81.90	-35.49	-159.53	-1.14	131.34
2.8	-7.64	140.90	2.76	-94.52	-36.42	169.67	-1.00	128.53
2.9	-5.46	132.74	1.73	-107.17	-38.64	141.86	-0.83	125.80
3	-3.98	123.58	0.55	-119.21	-36.59	118.45	-0.98	121.71

Application Circuit PC Board Layout



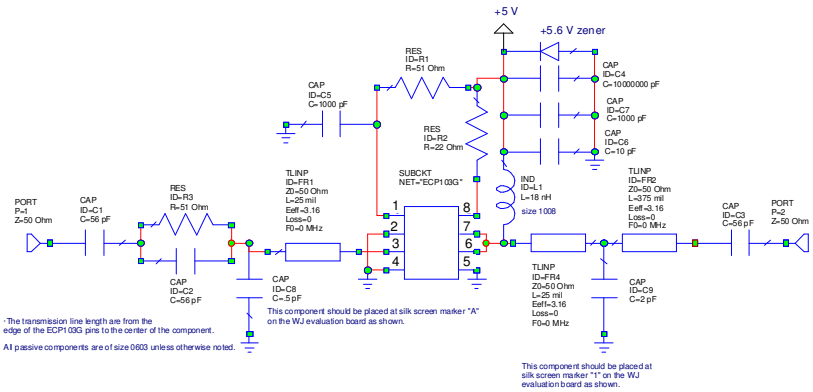
Circuit Board Material: Top RF layer is .014” Getek, 4 total layers (0.062” thick) for mechanical rigidity
1 oz copper, Microstrip line details: width = .026”, spacing = .026”
The silk screen markers ‘A’, ‘B’, ‘C’, etc. and ‘1’, ‘2’, ‘3’, etc. are used as placemarkers for the input and output tuning shunt capacitors – C8 and C9. The markers and vias are spaced in .050” increments.

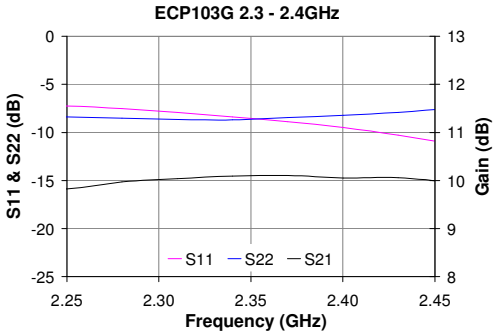
2350 MHz Reference Design

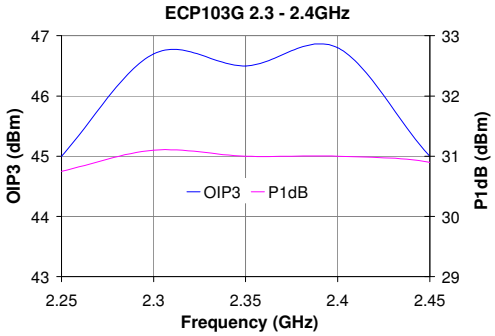
Typical RF Performance at 25°C

Frequency	2350 MHz
S21 – Gain	10 dB
S11 – Input Return Loss	-8.5 dB
S22 – Output Return Loss	-8.5 dB
Output P1dB	+31 dBm
Output IP3 (+15 dBm / tone, 1 MHz spacing)	+47.5 dBm
Noise Figure	6.3 dB
Device / Supply Voltage	+5 V
Quiescent Current (1)	450 mA

1. This corresponds to the quiescent current or operating current under small-signal conditions into pins 6, 7, and 8.





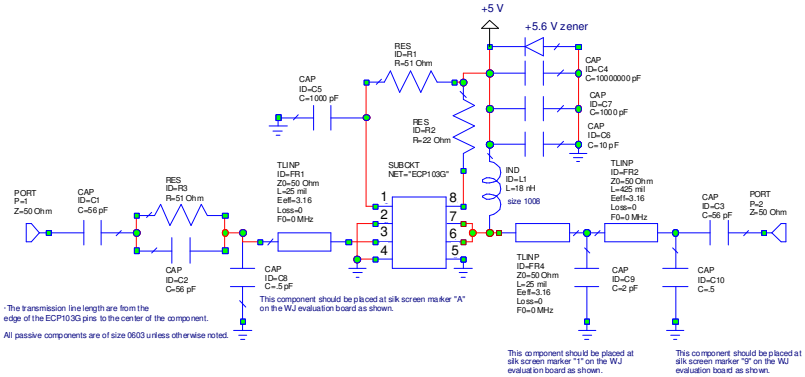


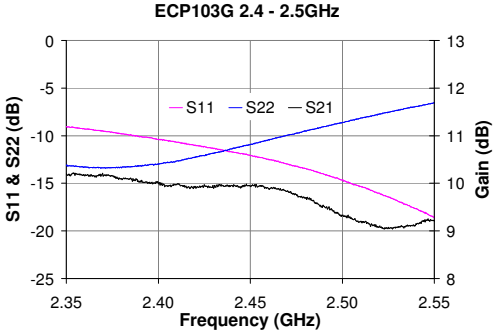
2450 MHz Application Circuit (ECP103G-PCB2450)

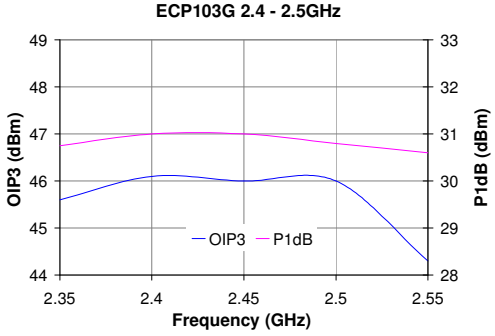
Typical RF Performance at 25°C

Frequency	2450 MHz
S21 – Gain	10 dB
S11 – Input Return Loss	-12 dB
S22 – Output Return Loss	-11 dB
Output P1dB	+30.5 dBm
Output IP3 (+15 dBm / tone, 1 MHz spacing)	+46 dBm
Noise Figure	6.3 dB
Device / Supply Voltage	+5 V
Quiescent Current (1)	450 mA

1. This corresponds to the quiescent current or operating current under small-signal conditions into pins 6, 7, and 8.





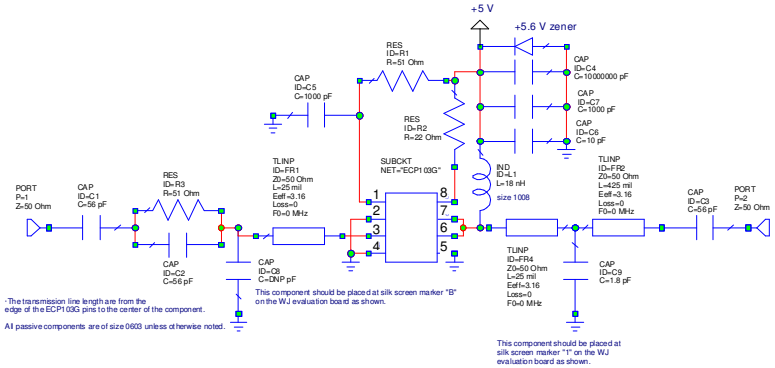


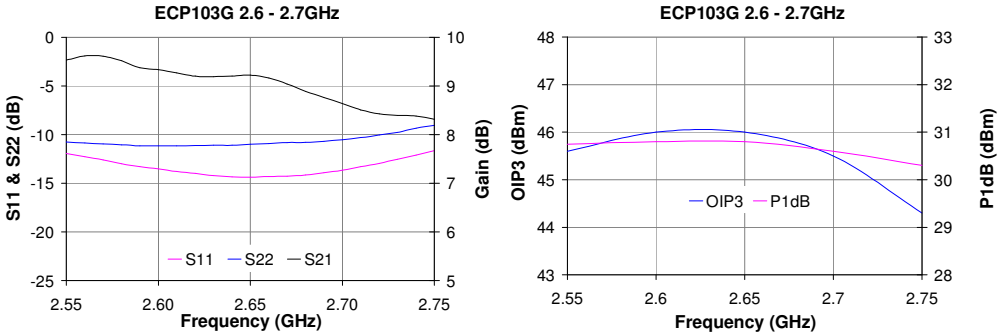
2650 MHz Application Circuit (ECP103G-PCB2650)

Typical RF Performance at 25°C

Frequency	2650 MHz
S21 – Gain	9 dB
S11 – Input Return Loss	-14 dB
S22 – Output Return Loss	-11 dB
Output P1dB	+30.5 dBm
Output IP3 (+15 dBm / tone, 1 MHz spacing)	+46 dBm
Noise Figure	6.3 dB
Device / Supply Voltage	+5 V
Quiescent Current (1)	450 mA

1. This corresponds to the quiescent current or operating current under small-signal conditions into pins 6, 7, and 8.

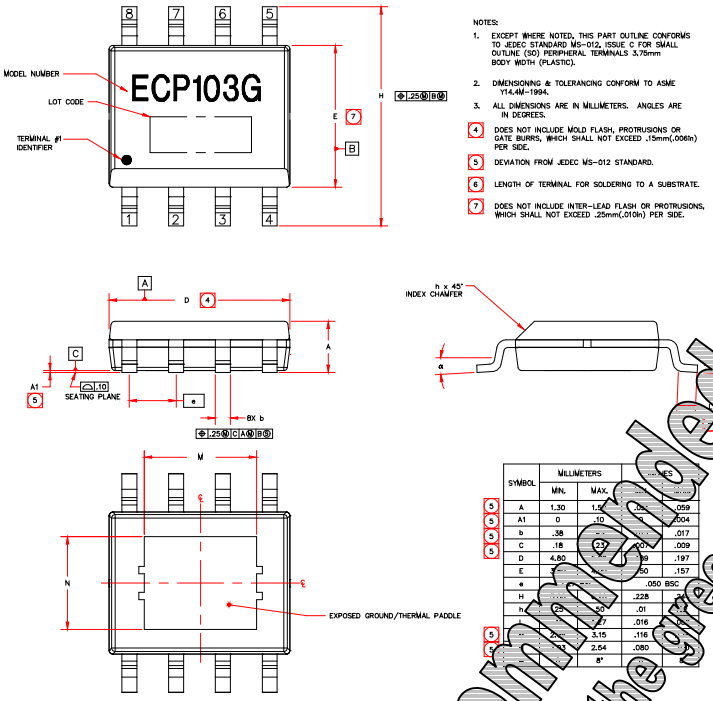




ECP103G (SOIC-8 Package) Mechanical Information

This package may contain lead-bearing materials. The plating material on the leads is SnPb.

Outline Drawing



Product Marking

The component will be marked with an "ECP103" designator and an alphanumeric lot code on the top surface of the package.

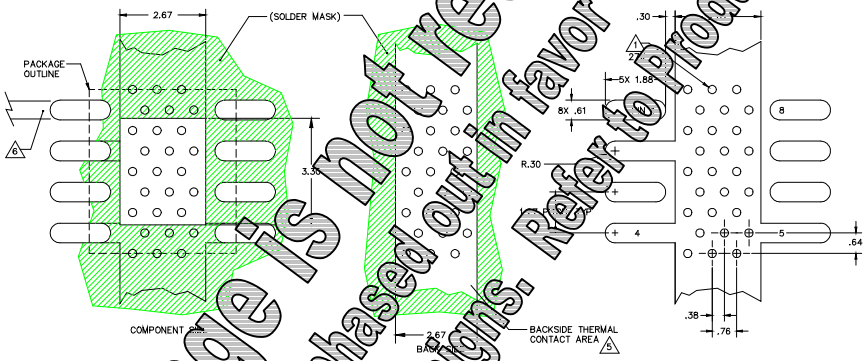
Tape and reel specifications for this part are located on the website in the "Application Notes" section.

ESD / MSL Information

Caution! ESD sensitive device.

ESD Rating:	Class 1B
Value:	Passes between 500 and 1000V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114
MSL Rating:	Level 3 at +235° C convection reflow
Standard:	JEDEC Standard J-STD-020

Land Pattern



Mounting Config. Notes

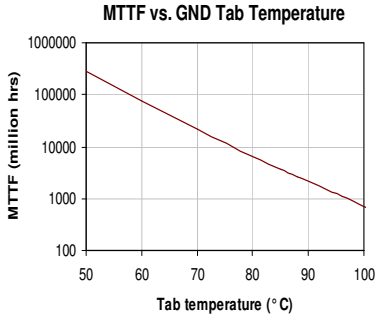
1. A heatsink underneath the area of the PCB for the mounted device is strictly required for proper thermal operation. Damage to the device can occur without the use of one.
2. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
3. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
4. Mounting screws can be added near the part to fasten the board to a heatsink. Ensure that the ground / thermal via region contacts the heatsink.
5. Do not put solder mask on the backside of the PC board in the region where the board contacts the heatsink.
6. RF trace width depends upon the PC board material and construction.
7. Use 1 oz. Copper minimum.
8. All dimensions are in millimeters (inches). Angles are in degrees.

Thermal Specifications

Parameter	Rating
Operating Case Temperature	-40 to +85° C
Thermal Resistance, Rth (1)	42° C / W
Junction Temperature, Tjc (2)	239° C

Notes:

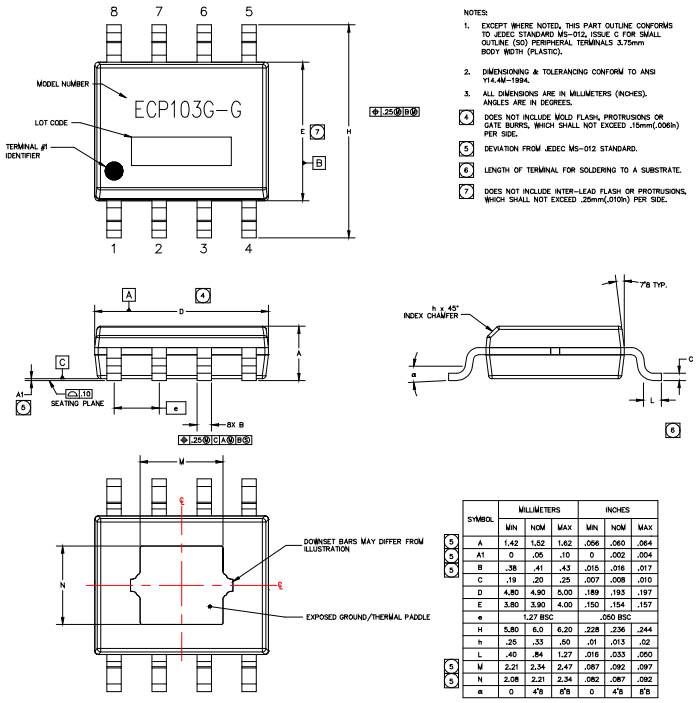
1. The thermal resistance is referenced from the junction-to-case at a case temperature of 85° C. Tjc is a function of the voltage at pins 6 and 8 and the current applied to pins 6, 7, 8 only and can be calculated by:
   Tjc = Tcase + Rth * Vcc * Icc
2. This corresponds to typical biasing condition of +5V, 450 mA at an 85° C case temperature. A minimum MTTF of 1 million hours is achieved for junction temperatures below 247° C.



ECP103G-G (Lead-Free Package) Mechanical Information

This package is lead-free/green/RoHS-compliant. The plating material on the leads is NiPdAu. It is compatible with both lead-free (maximum 260°C reflow temperature) and lead (maximum 245°C reflow temperature) soldering processes.

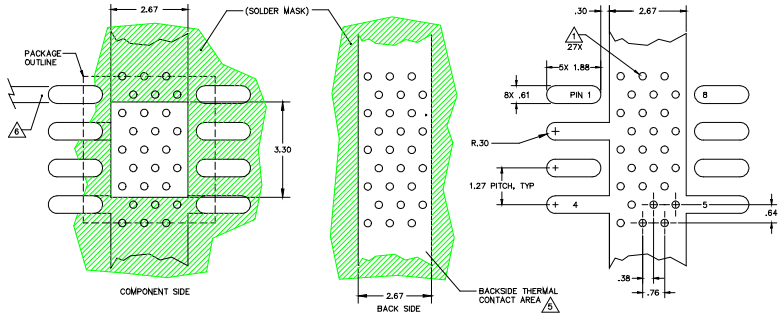
Outline Drawing



NOTES:
1. EXCEPT WHERE NOTED, THIS PART OUTLINE CONFORMS TO JEDEC STANDARD MS-012, ISSUE C FOR SMALL OUTLINE (SO) PERIPHERAL TERMINALS 3.75mm BODY WIDTH (PLASTIC).
2. DIMENSIONING & TOLERANCING CONFORM TO ANSI Y14.5M-1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS (INCHES). ANGLES ARE IN DEGREES.
4. DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS, WHICH SHALL NOT EXCEED .15mm(.006in) PER SIDE.
5. DEVIATION FROM JEDEC MS-012 STANDARD.
6. LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
7. DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS, WHICH SHALL NOT EXCEED .25mm(.010in) PER SIDE.

SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.42	1.52	1.62	.056	.060	.064
A1	0	.05	.10	0	.002	.004
B	.38	.41	.43	.015	.016	.017
C	.19	.20	.25	.007	.008	.010
D	4.80	4.90	5.00	.189	.193	.197
E	3.80	3.90	4.00	.150	.154	.157
e	1.27 BSC			.050 BSC		
H	5.80	6.0	6.20	.228	.236	.244
h	.25	.33	.50	.01	.013	.02
L	.40	.84	1.27	.016	.033	.050
W	2.21	2.34	2.47	.087	.092	.097
N	2.08	2.21	2.34	.082	.087	.092
α	0	4°ß	8°ß	0	4°ß	8°ß

Mounting Configuration / Land Pattern



Product Marking

The component will be marked with an "ECP103G-G" designator with an alphanumeric lot code on the top surface of the package.

Tape and reel specifications for this part are located on the website in the "Application Notes" section.

ESD / MSL Information

Caution! ESD sensitive device.

ESD Rating:	Class 1B
Value:	Passes ⩾ 500 V to <1000 V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114
MSL Rating:	Level 2 at +260 °C convection reflow
Standard:	JEDEC Standard J-STD-020

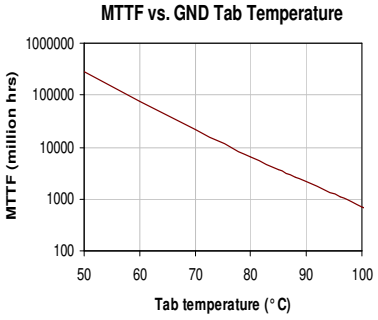
Mounting Config. Notes

1. A heatsink underneath the area of the PCB for the mounted device is strictly required for proper thermal operation. Damage to the device can occur without the use of one.
2. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
3. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
4. Mounting screws can be added near the part to fasten the board to a heatsink. Ensure that the ground / thermal via region contacts the heatsink.
5. Do not put solder mask on the backside of the PC board in the region where the board contacts the heatsink.
6. RF trace width depends upon the PC board material and construction.
7. Use 1 oz. Copper minimum.
8. All dimensions are in millimeters (inches). Angles are in degrees.

Thermal Specifications

Parameter	Rating
Operating Case Temperature	-40 to +85° C
Thermal Resistance, Rth (1)	33° C / W
Junction Temperature, Tjc (2)	159° C

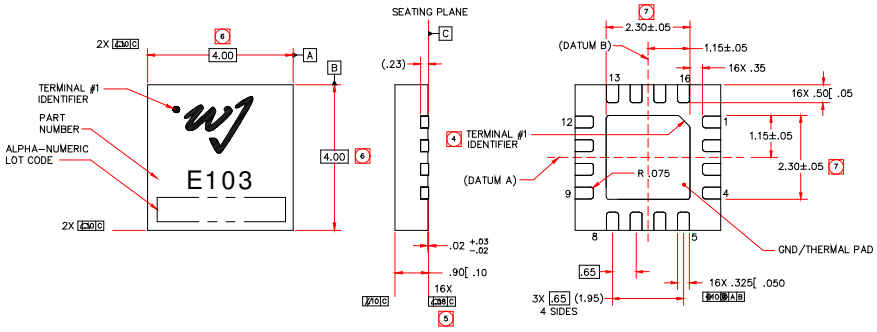
Notes:
1. The thermal resistance is referenced from the junction-to-case at a case temperature of 85° C. Tjc is a function of the voltage at pins 6 and 7 and the current applied to pins 6, 7, and 8 and can be calculated by:
   Tjc = Tcase + Rth * Vcc * Icc
2. This corresponds to the typical biasing condition of +5V, 450 mA at an 85° C case temperature. A minimum MTTF of 1 million hours is achieved for junction temperatures below 247° C.



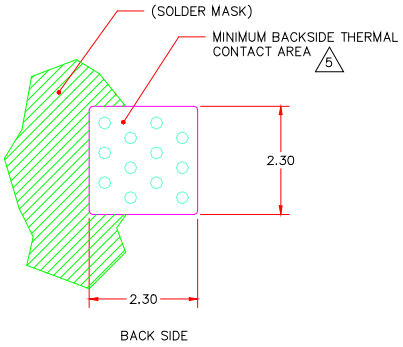
ECP103D (16-pin 4x4mm Package) Mechanical Information

This package may contain lead-bearing materials. The plating material on the leads is SnPb.

Outline Drawing



Land Pattern



Product Marking

The component will be marked with an "E103" designator with an alphanumeric lot code on the top surface of the package.

Tape and reel specifications for this part are located on the website in the "Application Notes" section.

ESD / MSL Information

Caution! ESD sensitive device.

ESD Rating:	Class 1B
Value:	Passes between 500 and 1000V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114
MSL Rating:	Level 3 at +235° C convection reflow
Standard:	JEDEC Standard J-STD-020

Mounting Config. Notes

1. A heatsink underneath the area of the PCB for the mounted device is strictly required for proper thermal operation. Damage to the device can occur without the use of one.
2. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
3. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
4. Mounting screws can be added near the part to fasten the board to a heatsink. Ensure that the ground / thermal via region contacts the heatsink.
5. Do not put solder mask on the backside of the PC board in the region where the board contacts the heatsink.
6. RF trace width depends upon the PC board material and construction.
7. Use 1 oz. Copper minimum.
8 All dimensions are in millimeters. Angles are in degrees.

Thermal Specifications

Parameter	Rating
Operating Case Temperature	-40 to +85° C
Thermal Resistance, Rth (1)	33° C / W
Junction Temperature, Tjc (2)	159° C

Notes:

1. The thermal resistance is referenced from the junction-to-case at a case temperature of 85° C. Tjc is a function of the voltage at pins 10 and 11 and the current applied to pins 10, 11, and 16 and can be calculated by:
   Tjc = Tcase + Rth * Vcc * Icc
2. This corresponds to the typical biasing condition of +5V, 450 mA at an 85° C case temperature. A minimum MTTF of 1 million hours is achieved for junction temperatures below 247° C.